WHAT IS CLAIMED IS:

1. A MOS transistor comprising:

an isolation layer formed at a predetermined region of a semiconductor substrate to define an active region;

an upper trench region formed in the active region, the upper trench region crossing the active region to divide the active region into two sub-active regions;

a spacer covering at least a pair of sidewalls of the upper trench region that are adjacent to the active region;

a lower trench region formed under the upper trench region surrounded by the spacer;

a pair of high concentration source/drain regions formed at top surfaces of the sub-active regions that are located at both sides of the upper trench region respectively;

a gate insulating layer covering the sidewalls and a bottom surface of the lower trench region; and

a gate electrode filling the lower trench region, surrounded by the gate insulating layer, and filling the upper trench region, surrounded by the spacer.

2. The MOS transistor of claim 1, wherein the upper trench region has a greater width than the active region.

3. The MOS transistor of claim 1, wherein the spacer comprises a first spacer adjacent to the active region and a second spacer adjacent to the isolation layer, the first spacer having the same width as the second spacer.

4. The MOS transistor of claim 3, wherein the upper trench region has a width that is equal to or greater than the sum of twice width of the second spacer and the width of the active region

5. The MOS transistor of claim 3 further comprising a pair of low concentration source/drain regions formed in the semiconductor substrate under the first spacer, and formed in contact with sidewalls of the lower trench region.

6. The MOS transistor of claim 1, wherein the lower trench region has the same width as the active region.

7. A method of fabricating a MOS transistor comprising:

forming an isolation layer at a predetermined region of a semiconductor substrate to define an active region;

etching a predetermined region of the active region to form an upper trench region that crosses the active region, the upper trench region dividing the active region into two sub-active regions;

forming a spacer on sidewalls of the upper trench region that are adjacent to the sub-active regions;

selectively etching the semiconductor substrate in the upper trench region using the spacer as an etching mask to form a lower trench region under the upper trench region;

forming a gate insulating layer on sidewalls and a bottom surface of the lower trench region;

forming a gate electrode that fills the lower trench region, surrounded by the gate insulating layer, and that fills the upper trench region, surrounded by the spacer; and

forming a pair of high concentration source/drain regions at top surfaces of the sub-active regions that are located at both sides of the upper trench region respectively.

8. The method of claim 7, wherein forming the upper trench region comprises:

sequentially forming a pad oxide layer and a pad nitride layer on an entire surface of the substrate having the isolation layer;

patterning the pad nitride layer to form an opening that crosses over the active region;

successively etching the pad oxide layer and the semiconductor substrate using the pad nitride layer as an etching mask; and

removing the patterned pad nitride layer, the spacer being formed on sidewalls of the upper trench region and the etched pad oxide layer.

9. The method of claim 8, wherein the opening is formed to have a greater width than the active region.

10. The method of claim 7 further comprising forming a low concentration impurity layer under a bottom surface of the upper trench region prior to formation of the

spacer, the low concentration impurity layer having a different conductivity type from the semiconductor substrate.

11. The method of claim 7, wherein forming the spacer comprises:

forming a conformal spacer insulating layer on an entire surface of the substrate having the upper trench region; and

anisotropically etching the spacer insulating layer to form a pair of first spacers adjacent to the active region and a pair of second spacers adjacent to the isolation layer, a distance between the second spacers is equal to or greater than the width of the active region.

12. The method of claim 11, wherein the spacer insulating layer is formed of a silicon oxide layer or a silicon nitride layer.

13. The method of claim 10, wherein the lower trench region is formed to be deeper than the low concentration impurity layer, to leave a pair of low concentration source/drain regions that are separated from each other and are located at both sides of the lower trench region.

14. The method of claim 7, wherein the lower trench region is formed to have the same width as the active region.

15. The method of claim 7, wherein forming the gate electrode comprises:

forming a gate conductive layer on an entire surface of the substrate including the gate insulating layer; and

patterning the gate conductive layer to form a gate conductive layer pattern that fills the upper and lower trench regions and crosses the active region.